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TITLE: IDENTIFYING CLOCK SYNCHRONIZING METHOD IN DATA REPRODUCING DEVICE AND DATA REPRODUCING DEVICE

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INVENTOR-INFORMATION:

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ABSTRACT:

PROBLEM TO BE SOLVED: To accelerate and correct initial pull-in of an identifying clock phase by sharing a low frequency component containing a DC component generated from a regenerative signal after waveform equalized with the signal of a high frequency component generated from the regenerative signal before waveform equalized.

SOLUTION: A phase error is detected from the regenerative signal after waveform equalized by a digital FIR filter 13 by a digital clock phase error detection circuit 16, and a first phase **error signal** is outputted. The phase error is detected from the regenerative signal before waveform equalized outputted from an LPF 11 by an analog clock phase error detection circuit 21, and a second phase **error signal** is outputted. The signal cutting a first phase **error signal** frequency component by a high-band cut-off filter 18 is synthesized with the signal cutting a second phase **error signal** low frequency component by a low-band cut-off filter 22 by an adder 25. By imparting the **synthesized signal to a VCO** 29 as a control signal through a loop filter 26, the initial pull-in operation of the identifying clock phase is performed.